

**Sukkur Institute of Business Administration University**

Department of Electrical Engineering

Digital System Design Lab, Spring 21

**Name: Deepak Lal**

**CMS: 041-18-0030**

**Lab Report # 01:**

Instructor: Dr. Safeer Hyder

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| **Lab Report Rubrics (02 Marks)** | | |
| **S.No** | **Criterion** | **00 to 01 Marks** |
| 1 | Design/Implementation/Testing Accuracy |  |
| 2 | Coding style/Timely submission/Academic Integrity |  |
| Total Marks | |  |

**Lab Exercises:**

**Question (1)**

Design, and implement a 2-bit Comparator.

**a)** Create a truth table, then drive Boolean expressions and simplify the output expressions using K- maps. Submit the snapshots for handwritten work.

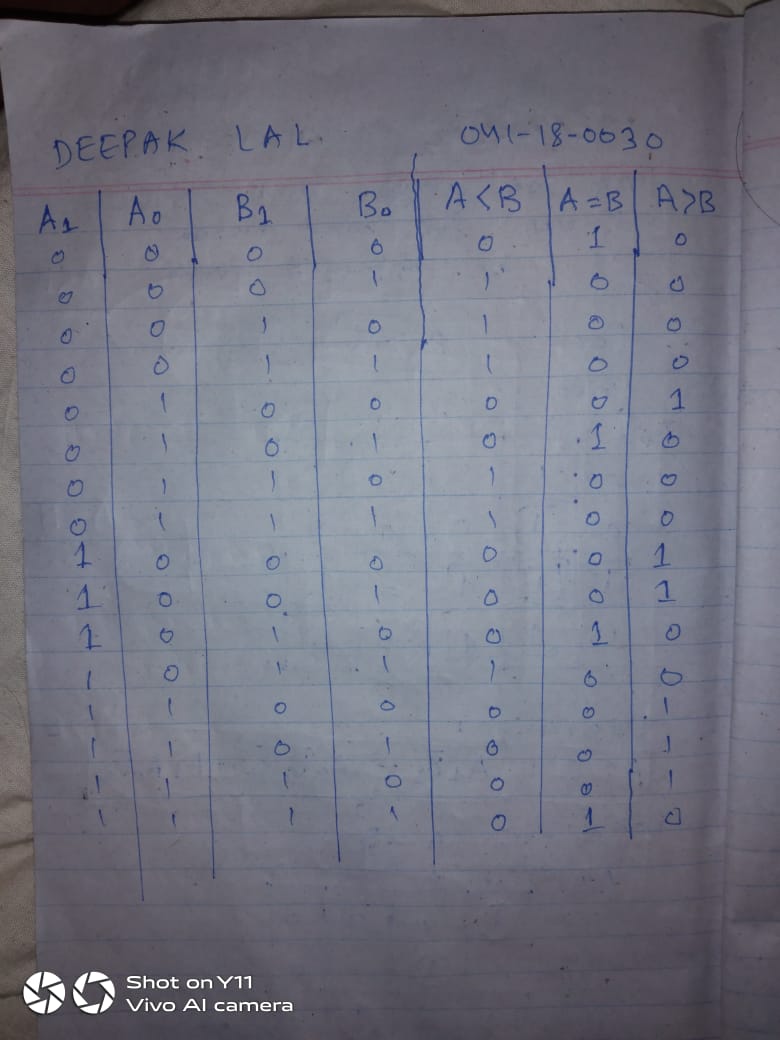
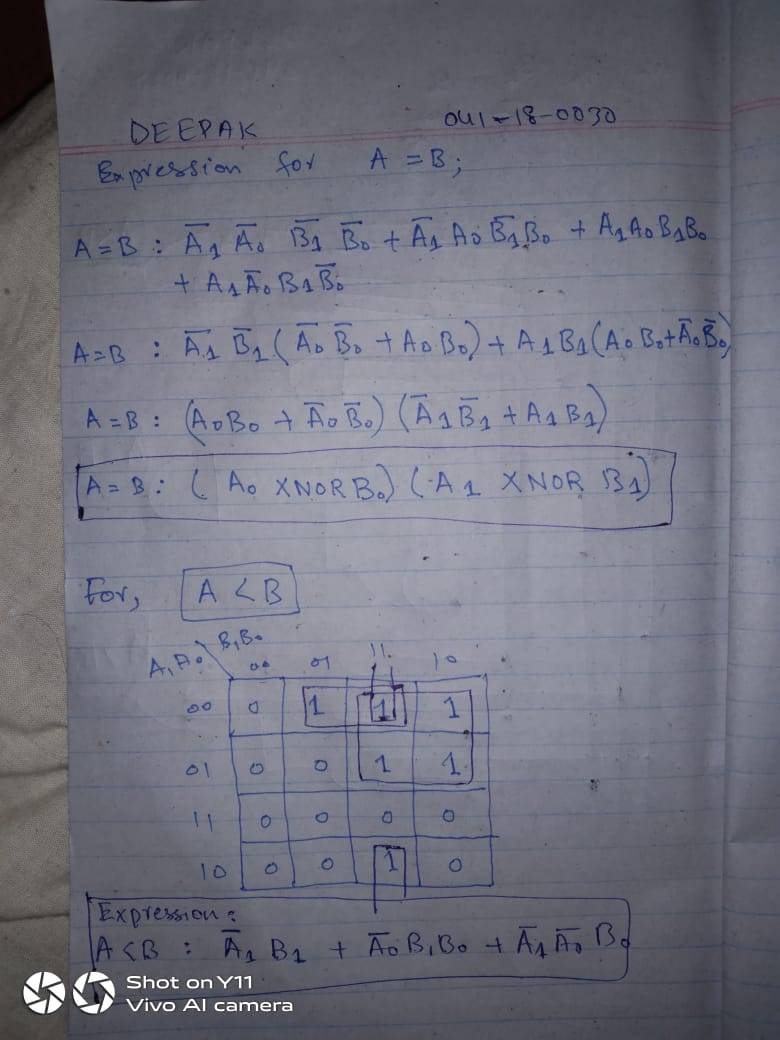
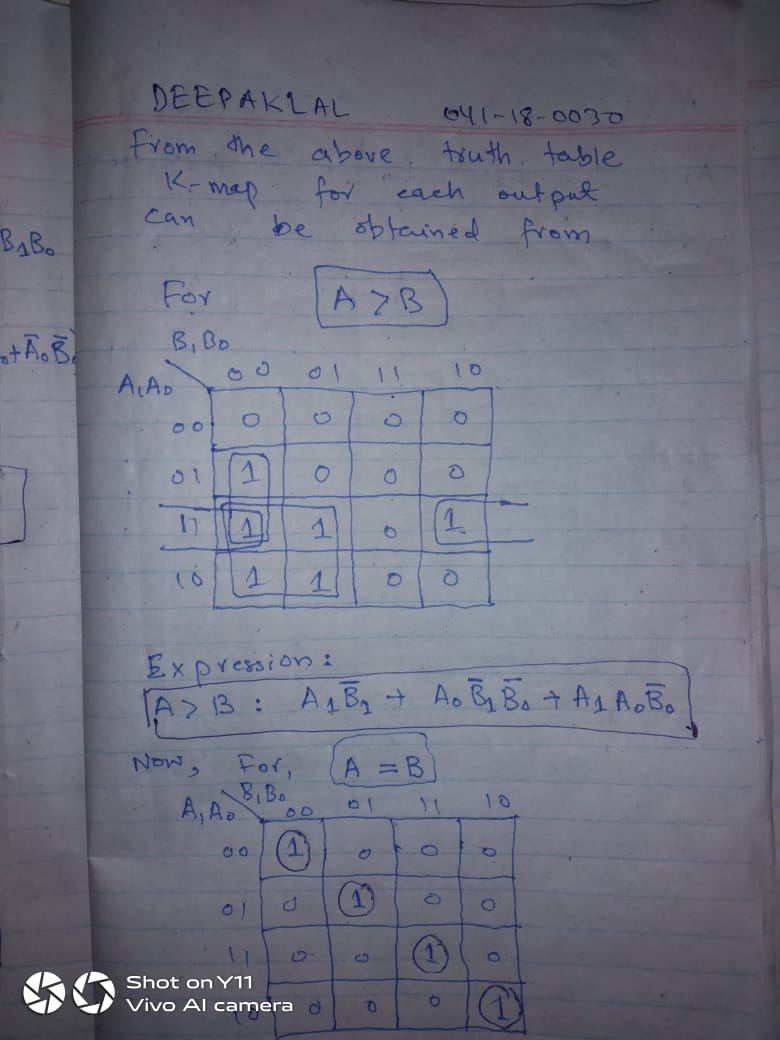
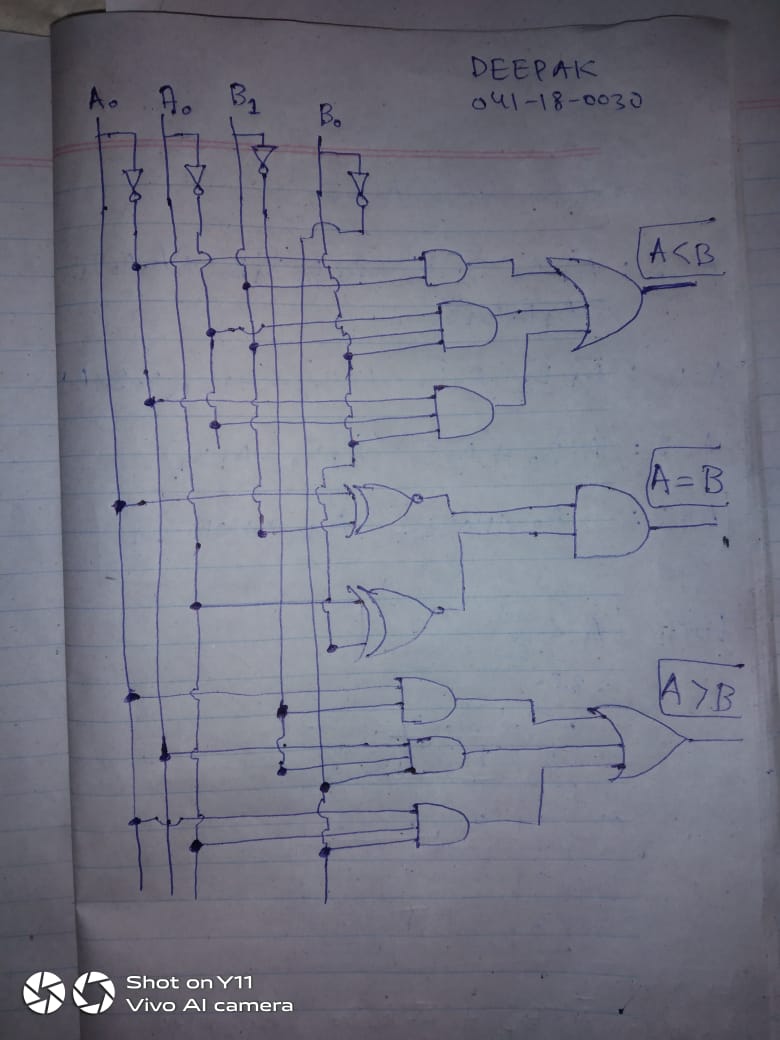
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Figure 1 Truth Table

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**b)** Implement the simplified design using Verilog gate-level modelling. Screenshot the codes and submit with the name signature.

**c)** Make sure codes are well commented with proper indentation.

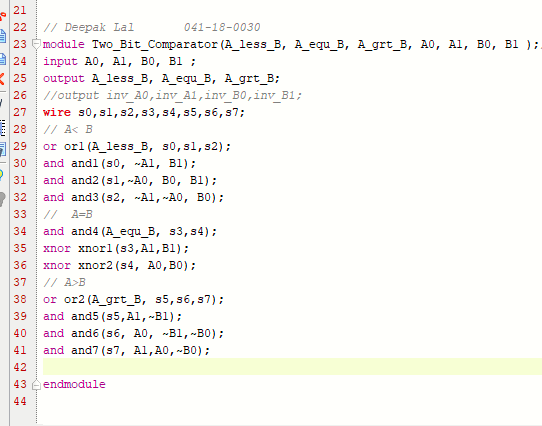


Figure 2 Design Source Code

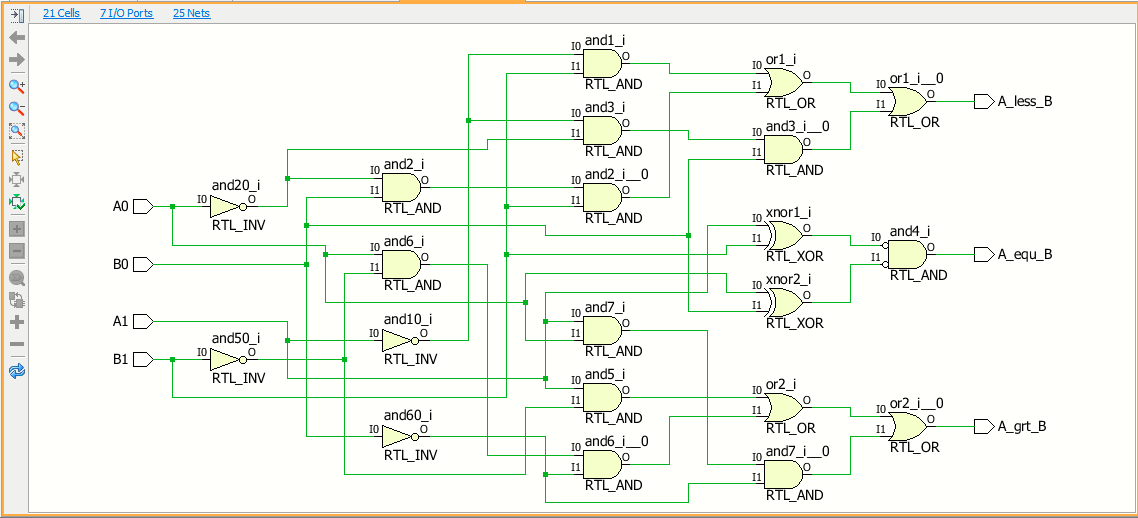
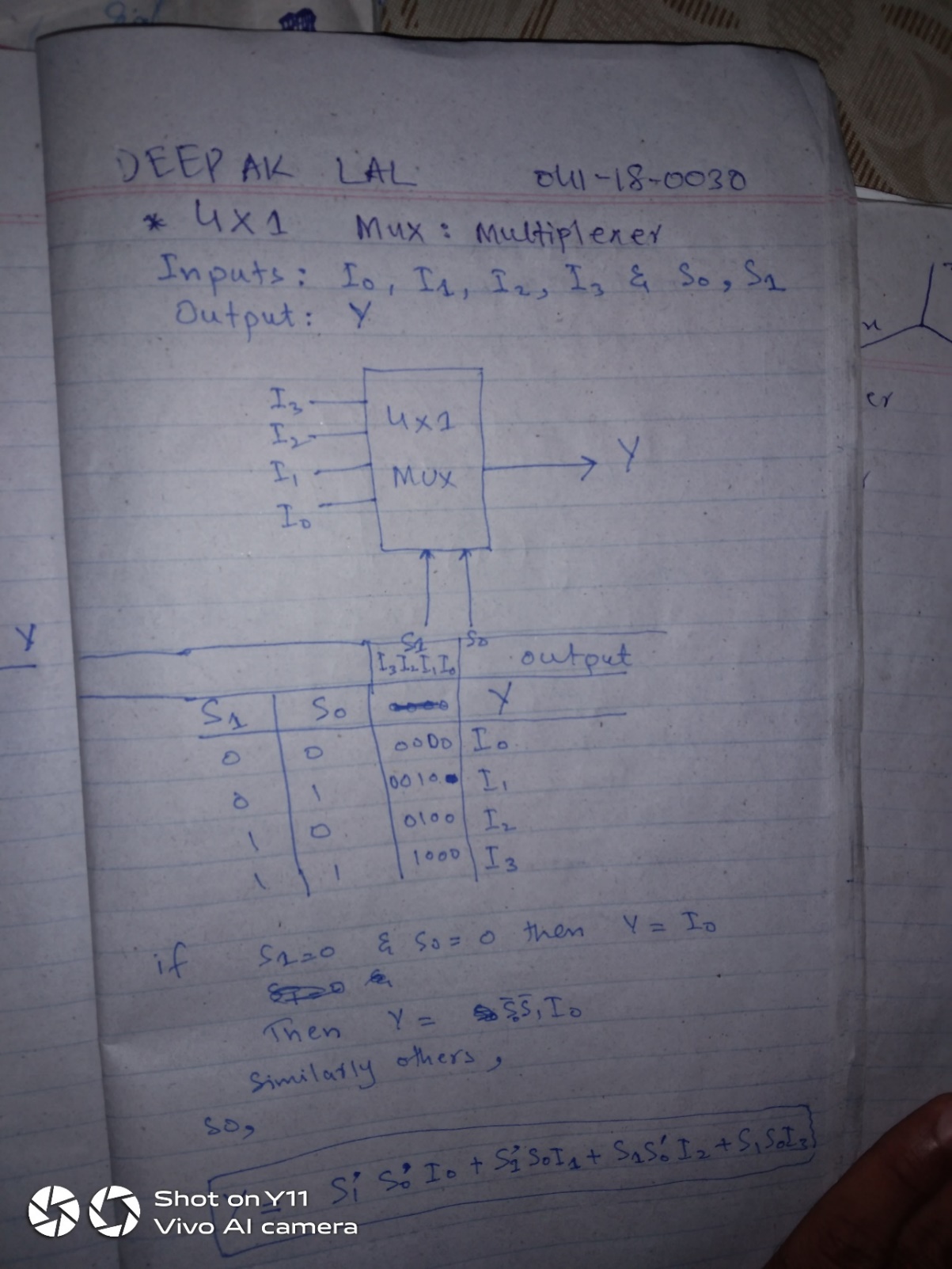


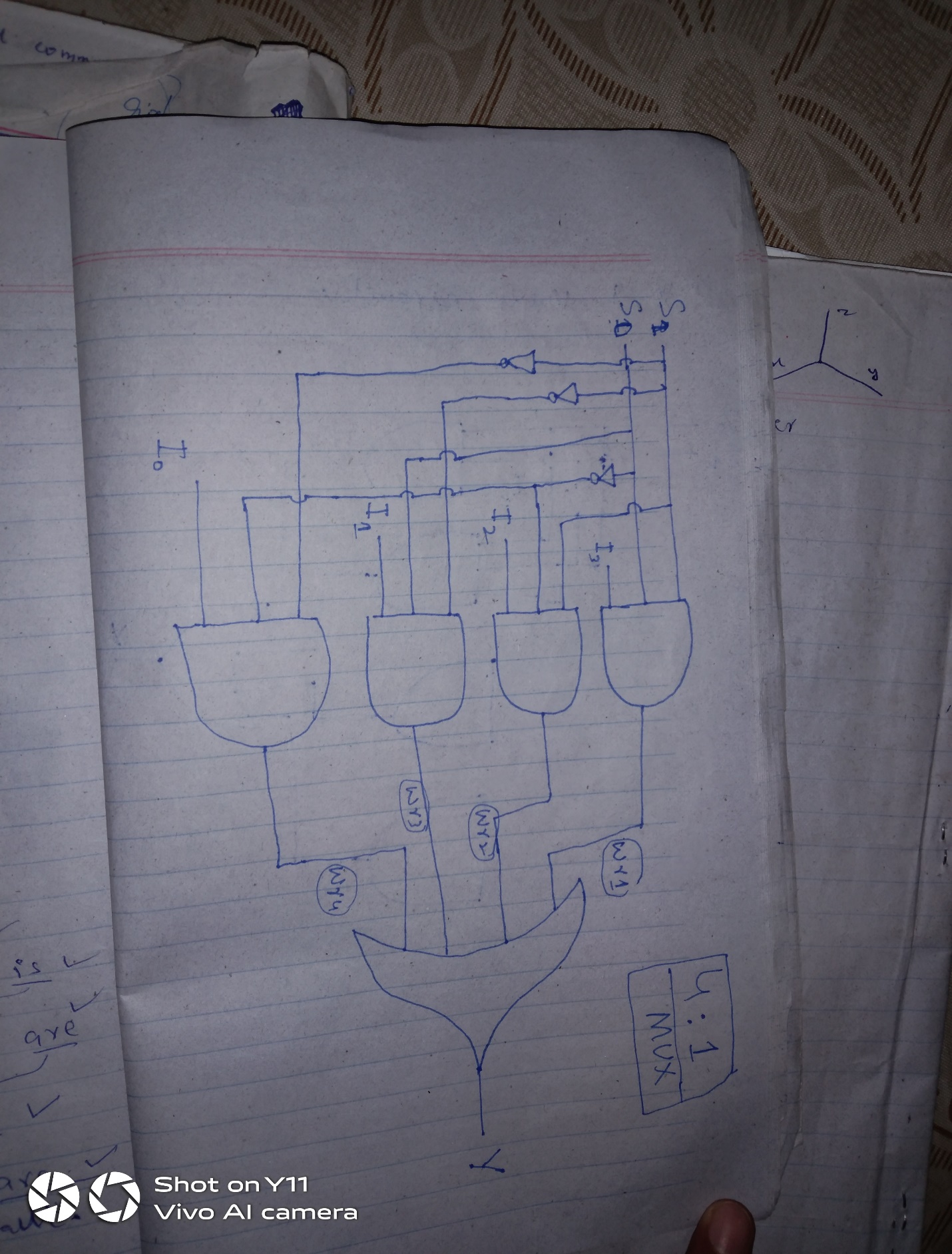
Figure 3 Schematic

**Question (1)**

Design, Implement, and test a 4-to-1 Multiplexer.

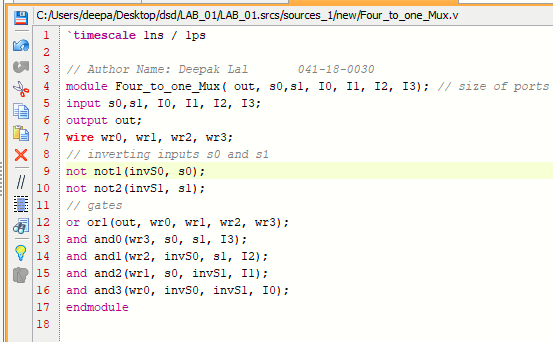
a) Create a truth table, then drive Boolean expressions. Submit the snapshots for handwritten work.

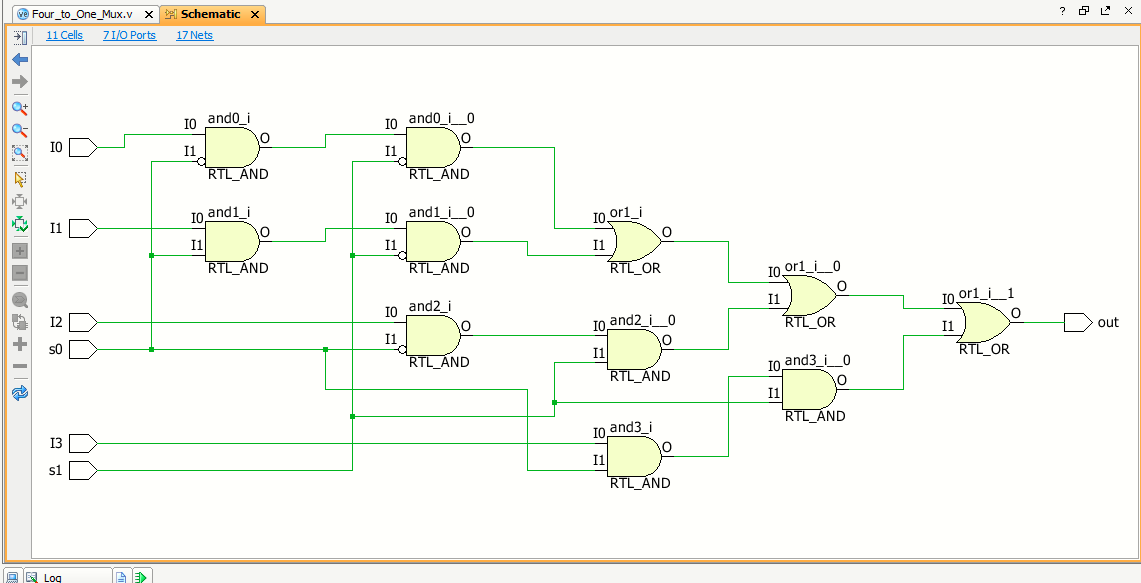




b) Implement the simplified design using Verilog gate-level modelling. Screenshot the codes and submit with the name signature.

c) Make sure codes are well commented with proper indentation.

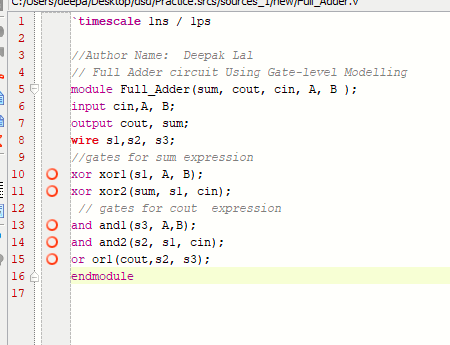




**Question 3)**

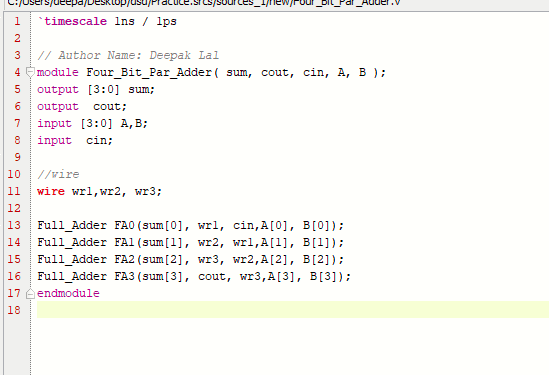
Design, Implement and investigate a 4-bit parallel adder by cascading four Full Adders.

1. Implement the Full Adder using gate-level modelling and test the design to make sure it is working. Submit the Verilog design and test bench code screenshots with name signatures. Also submit the tcl console and timing diagram outputs.

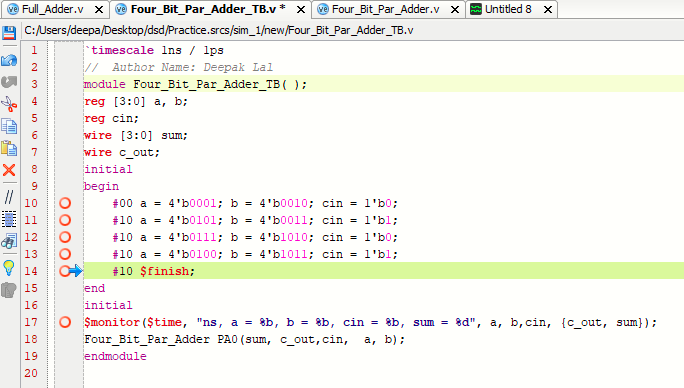


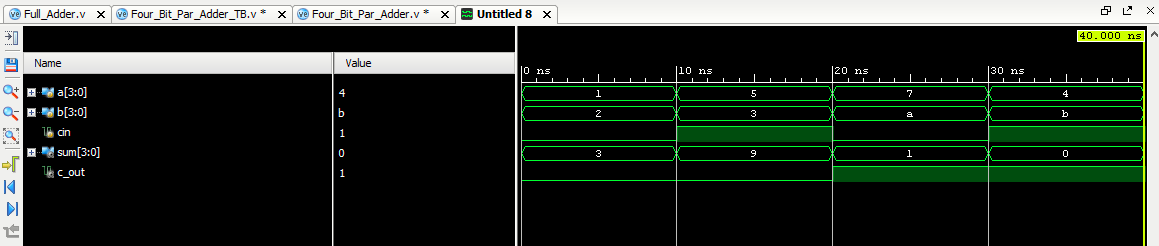
**Figure 4 Full Adder**

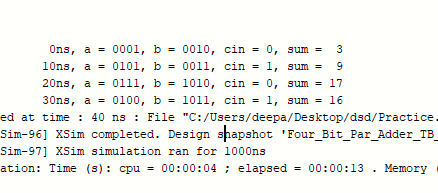
1. Implement the 4-bit adder by connecting pre-designed full adder modules. Submit the design codes screenshots with name signatures.



1. Test the design using Verilog test bench. Submit the test bench codes with name signatures along with the tcl console outputs and timing diagrams.



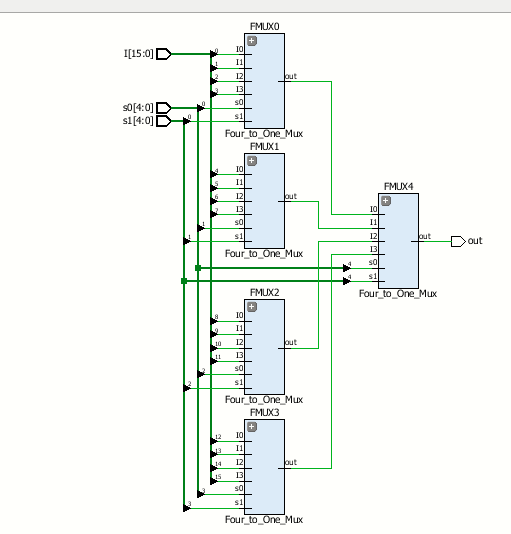


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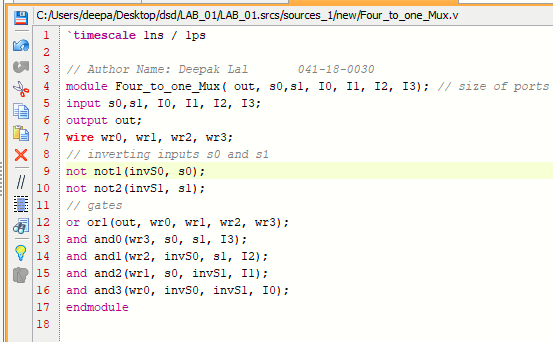
**Question 04)**

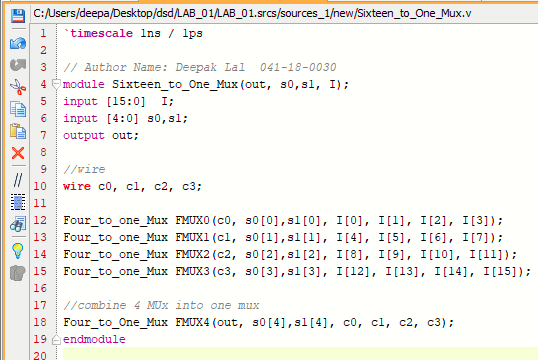
Design, implement and investigate a 16-to-1 multiplexer by interconnecting five 4-to-1 multiplexers using hierarchical modelling approach.

1. Provide the design with schematic diagram.

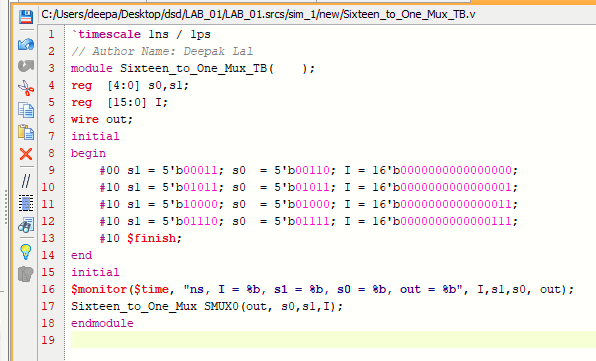


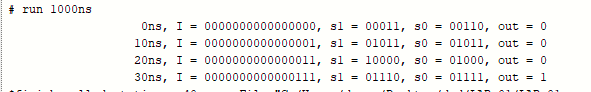
1. Implement the design using Verilog hierarchical modelling. Submit the design codes’ screenshots with name signatures.





1. Test the design using both testbench simulation. Submit the test bench codes with tcl console and timing diagrams. Make sure codes are properly commented.







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**Lab Report # 02:**

Instructor: Dr. Safeer Hyder

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| **Lab Report Rubrics (02 Marks)** | | |
| **S.No** | **Criterion** | **00 to 01 Marks** |
| 1 | Design/Implementation/Testing Accuracy |  |
| 2 | Coding style/Timely submission/Academic Integrity |  |
| Total Marks | |  |

**Question: 01**

A magnitude comparator checks if one number is greater than or equal to or less than another number. A 4-bit magnitude comparator takes two 4-bit numbers A, and B as input.

1. Drive Boolean expressions for the design. Provide the handwritten work.

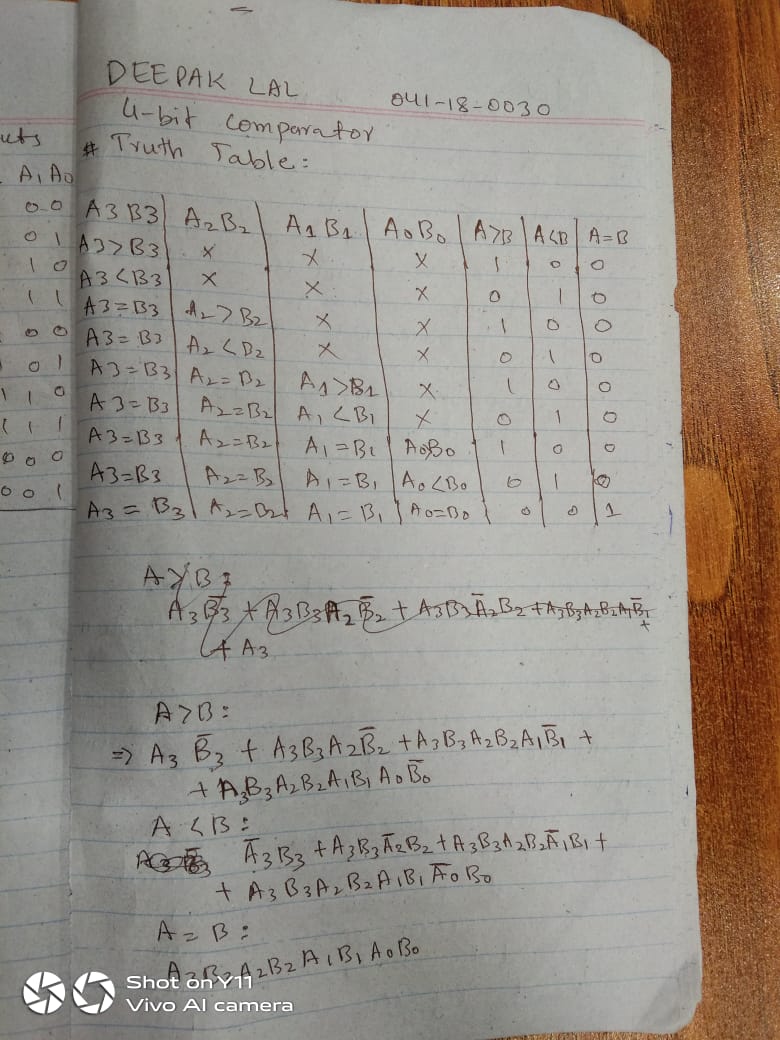
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Figure 5 Truth Table Of 4 Bit Comparator

1. Write the Verilog description of the module magnitude comparator using bitwise operators. Provide the codes with name signature.

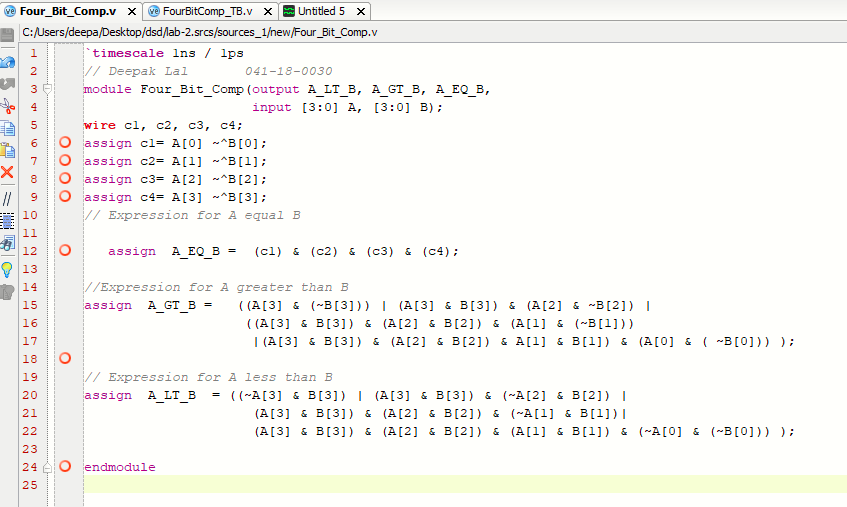


Figure 6 Verilog Design Source Code

1. Test the design using Verilog test bench. Provide the codes with the name signature, along with tcl console and timing diagram results. Make use of comments and indentations while coding.

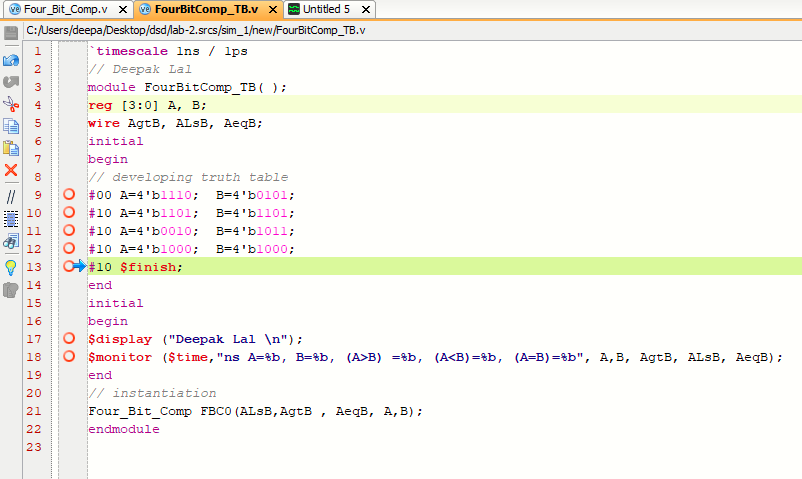
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Figure 7 Test Bench

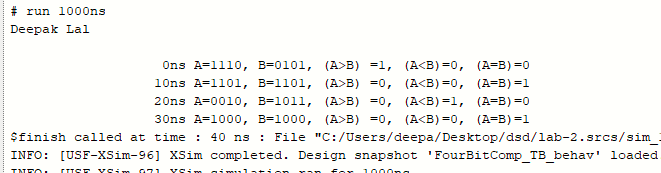


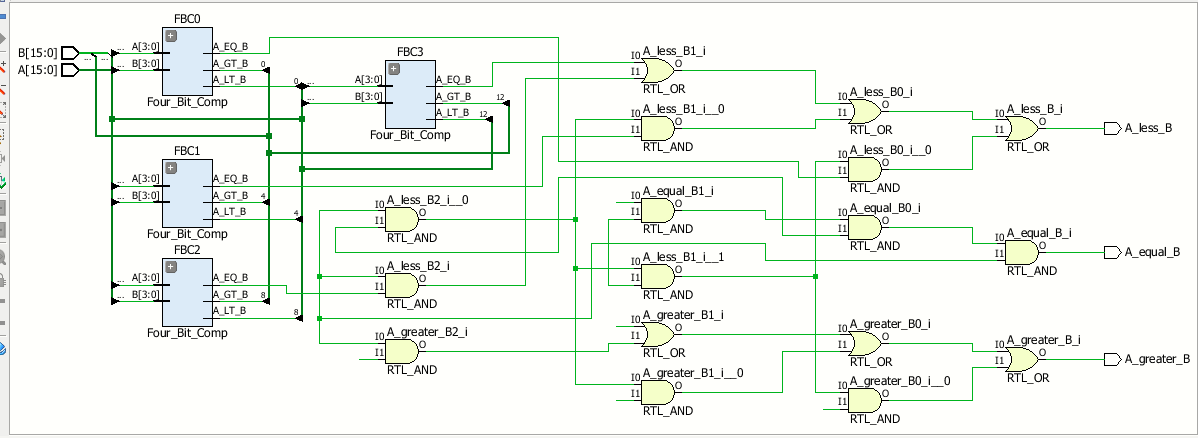
Figure 8 TCL Console

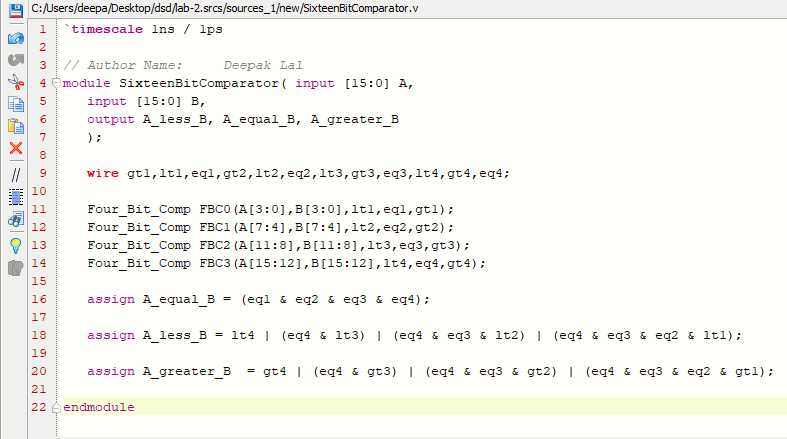
**Question 02:**

Design 16-bit comparator by cascading method.

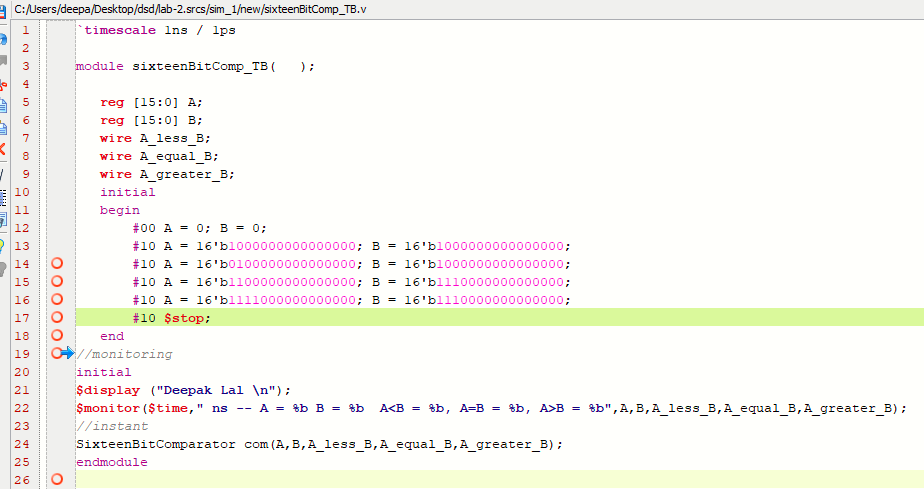
1. Provide the design schematic
2. Implement the design and provide the codes.
3. Write down the test bench and provide tcl console and timing diagrams. d. Make use of comments and indentations while coding.

**Schematic:**

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**Design Code: **

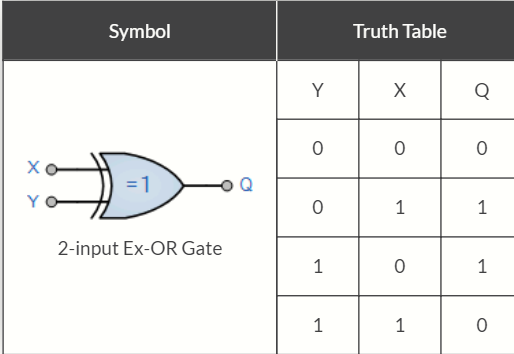
**Test Bench**

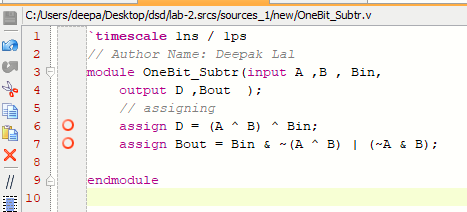
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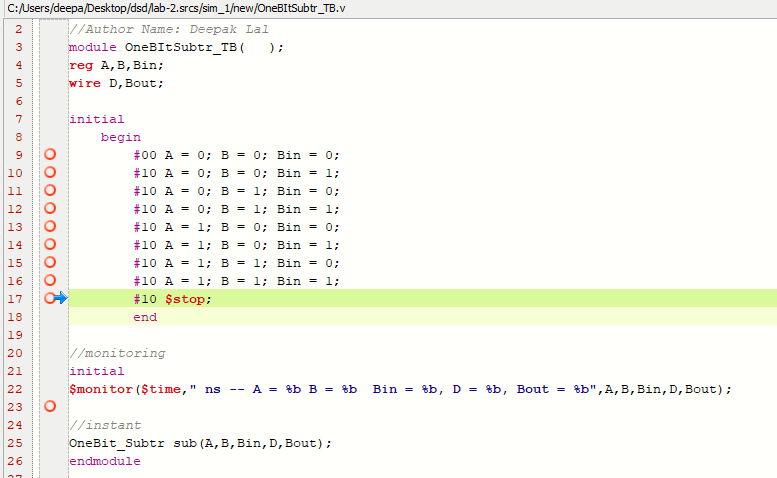
**Exercise Q 03:**

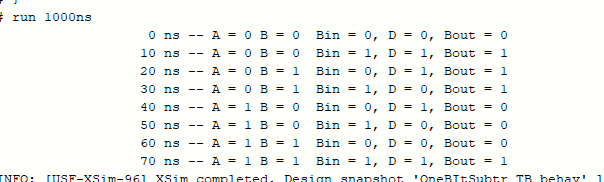
A full subtracter has three 1-bit inputs x,y, and z (previous borrow) and two 1-bit outputs D (difference) and B (borrow).

* Draw the truth table for the given circuit.
* Drive the simplified Boolean expression.
* Write the Verilog description for the subtractor module.
* Instantiate the design module in the test module and provide the tcl console and timing diagram outputs.

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**Lab Report # 03:**

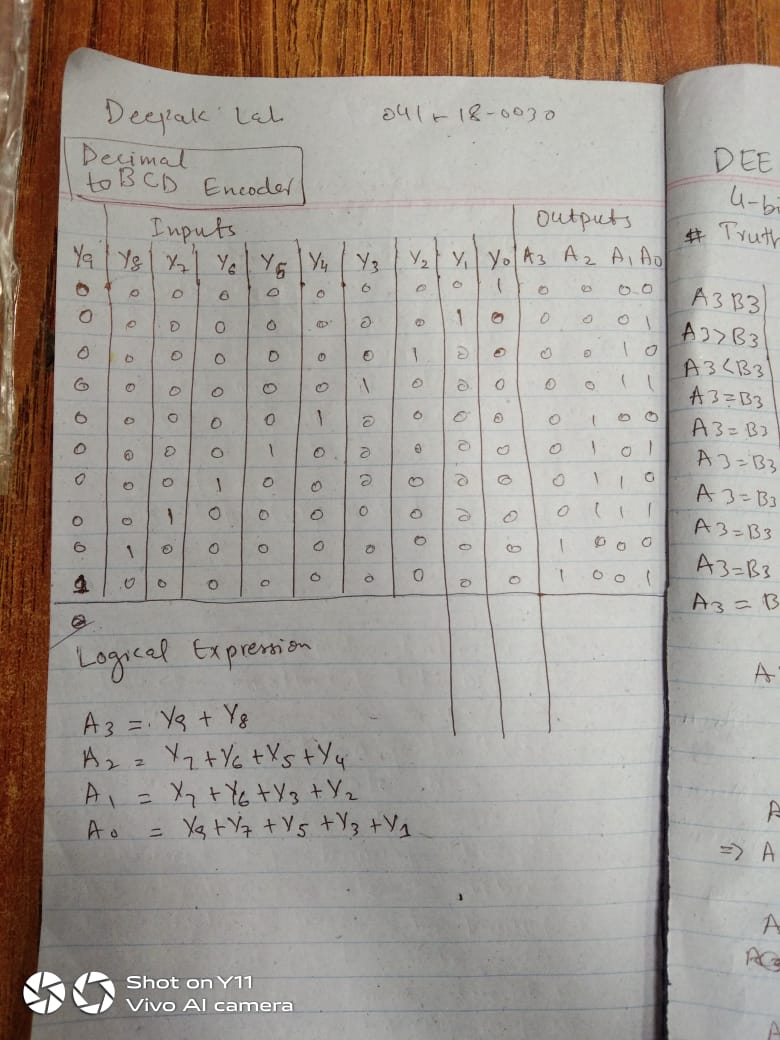
Instructor: Dr. Safeer Hyder

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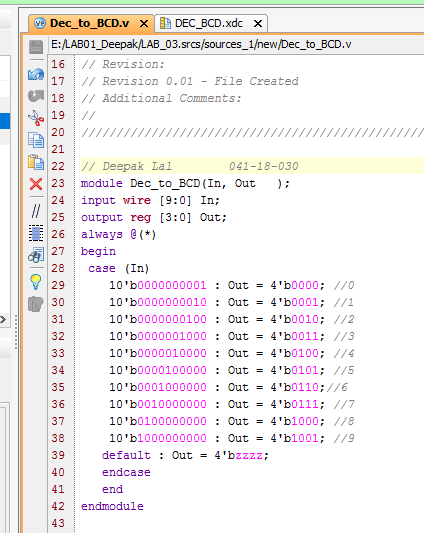
**Question 1**

Encoders are opposite to decoders, and are supposed to generate coded outputs from a single active numeric input. A Decimal to BCD Encoder takes 10 inputs and generates corresponding 4-bit outputs.

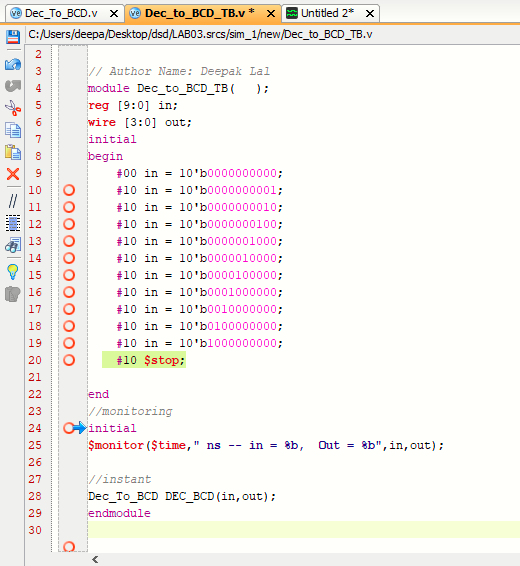
1. Design truth table for the decimal to BCD encoder. Derive the Boolean expression, and simplify if possible.



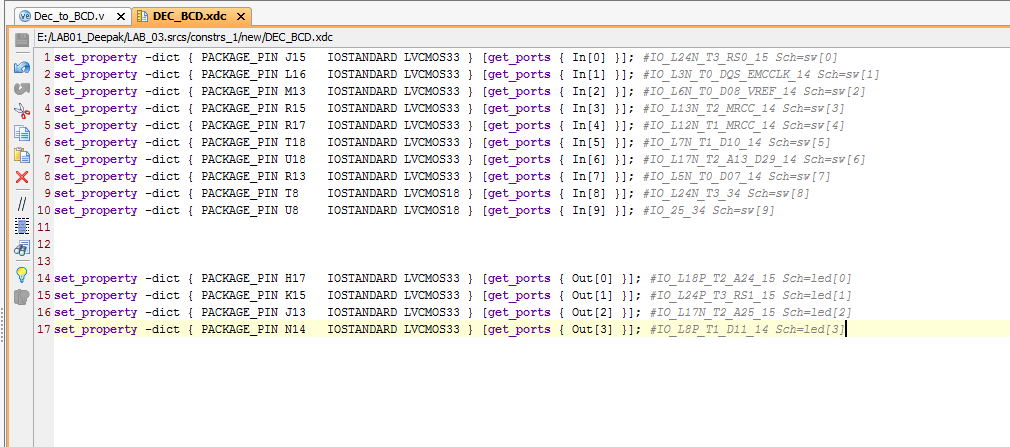
1. Implement the design using Verilog behavioral modelling, and provide code screenshot.

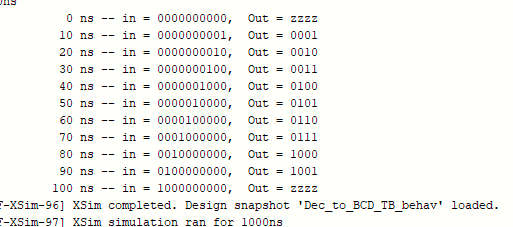


1. Investigate the design using Verilog test bench and simulations, and provide code screenshot.



1. Investigate the design using Nexys 4 DDR hardware. Provide the constraint file screenshot and hardware output image.



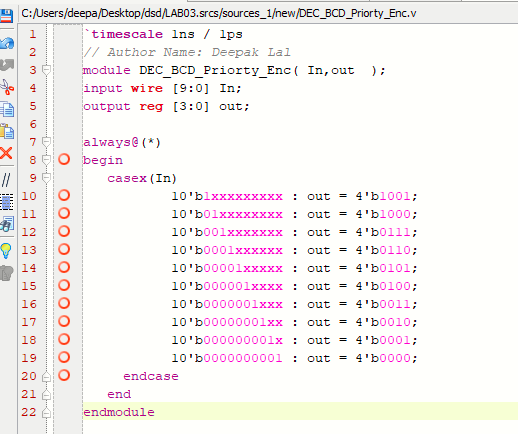


**Exercise Q 02:**

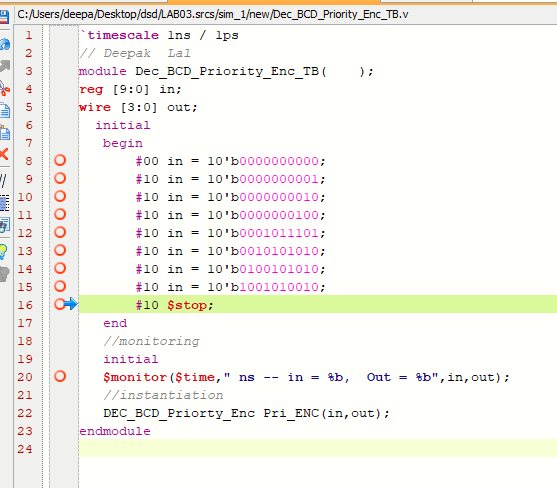
Conflict arises in encoders when more than two inputs are activated simultaneously. This issue can be resolved by prioritising the either LSB or MSB inputs. This encoder is called priority encoder. Redesign the above encoder and assign priority to the MSBs of the inputs. Hint: Make use of casex rather than case.

1. Design truth table for the decimal to BCD encoder.
2. Implement the design using Verilog behavioural modelling, and provide code screenshot.
3. Investigate the design using Verilog test bench and simulations, and provide code screenshot.
4. Investigate the design using Nexys 4 DDR hardware. Provide the constraint file screenshot and hardware output image.

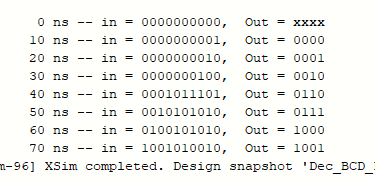
Design Code:



Test Bench:



Output console:



Timing diagram:

